

Amendments to the Specification:

Please replace paragraph [0011] with the following amended paragraph:

[0011] As described in greater detail below, an example semiconductor device includes a capacitor having a bottom electrode, a dielectric layer and an upper electrode, formed on a semiconductor substrate. The example semiconductor device also includes a first insulating layer formed on the semiconductor substrate to cover the capacitor, a plurality of first contact plugs formed in a plurality of first via holes of the first insulating layer, each of which is and electrically connected to the either the bottom electrode and/or the upper electrodes, a first metal wiring formed on the first insulating layer and electrically connected to the bottom electrode through the first contact plug, and a second contact plug formed on the first insulating layer and electrically connected to the upper electrode through the first contact plug. Still further, the example semiconductor device includes a second insulating layer formed on the first insulating layer to cover the first metal wiring and the second contact plug, an anti-fuse formed in a certain thickness in a second via hole of the second insulating layer and electrically connected to the second contact plug, a third contact plug filling the second via hole on the anti-fuse, and a second metal wiring formed on the second insulating layer and electrically connected to the third contact plug. Preferably, the first and second metal wirings are perpendicular to each other.

Please replace paragraph [0019] with the following amended paragraph:

[0019] Then, a first insulating layer 102 is formed on the semiconductor substrate including the upper electrode 100c. Successively, a photoresist (not shown) is coated on the first insulating layer 102, and the first insulating layer 102 is selectively etched and removed by a conventional photolithography process and an etching process. As a result, a plurality of first via holes 103 exposing the surfaces of the bottom and upper electrodes, is are formed by the selective etching of the first insulating layer 102.

Please replace paragraph [0021] with the following amended paragraph:

[0021] Then, as shown in Figure 5C, a metal layer for forming a first metal wiring is deposited on the first insulating layer 102 and on the first contact plug 104a, by using such as a sputtering process. Then, the metal layer for the first metal wiring is selectively patterned by a photolithography and an etching process, thus forming a first metal wiring 108a and a second contact plug 104 electrically connected to the different first contact plugs 104a, respectively.

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Response to the Office action of February 25, 2005

Please replace the abstract with the following amended abstract:

A semiconductor device having a variable capacitance capacitor and a method of manufacturing the same are disclosed. An example semiconductor device includes a capacitor having a bottom electrode, a dielectric layer and an upper electrode, formed on a semiconductor substrate. The example semiconductor also includes a first insulating layer formed on the semiconductor substrate to cover the capacitor, a plurality of a first contact plugs formed in a plurality of first via holes of the first insulating layer, each of which is and electrically connected to the either the bottom electrode and/or the upper electrodes, a first metal wiring formed on the first insulating layer and connected to the bottom electrode through the first contact plug, a second contact plug formed on the first insulating layer and connected to the upper electrode through the first contact plug, and a second insulating layer formed on the first insulating layer to cover the first metal wiring and the second contact plug. In addition, the example semiconductor device includes an anti-fuse formed in a certain thickness in a second via hole of the second insulating layer and electrically connected to the second contact plug, a third contact plug filling the second via hole on the anti-fuse, and a second metal wiring formed on the second insulating layer and electrically connected to the third contact plug.